II. CLAIM LISTING

1. (Currently Amended) A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit operable to store blocks of media data to be processed;

a second memory unit operable to store blocks of media data to be processed; and

a single instruction, multiple data (SIMD) processor operable to receive blocks of media data from the first and second memory units and to perform filtering operations on blocks of media data from the first and second memory units concurrently;

wherein the SIMD processor is operable to retrieve ~~the m most significant~~ less than all bits ~~of~~ stored in a first memory location in the first memory unit and ~~the n most significant~~ less than all bits ~~of~~ stored in a second memory location in the second memory unit, ~~where m is equal to one half of the number of bits stored in the first memory location and n is equal to one half of the number of bits stored in the second memory location,~~ and wherein the SIMD processor is operable to concurrently perform filtering operations on the [[m]] bits from the first memory location and the [[n]] bits from the second memory location.

2. (Previously Presented) The filter engine of claim 1 wherein the SIMD processor is adapted to receive blocks of data from the first and second memory units, and to concurrently perform filtering operations on blocks of data from the first and second memory units, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the SIMD processor is adapted to receive blocks of data from only one of the first and second memory units, and to perform filtering operations on the received blocks of data.

3-4. (cancelled)

5. (Previously Presented) The filter engine of claim 1 wherein the SIMD processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first memory unit while the second set of data path units is concurrently performing filtering operations on a block of data received from the second memory unit.

6. (Previously Presented) The filter engine of claim 5 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first memory unit while the second set of data path units concurrently performs filtering operations on a block of data received from the second memory unit, and wherein when the filter engine is in a non-split-operation mode, both the first and second sets of data path units perform filter operations on blocks of data from only one of the first and second memory units.

7-8. (cancelled)

9. (Previously Presented) The filter engine of claim 1 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein:

the first memory unit is adapted to store blocks of pixel data to be processed;

the second memory unit is adapted to store blocks of pixel data to be processed; and

the SIMD processor is adapted to receive blocks of pixel data from the first and second memory units and to perform filtering operations on blocks of pixel data from the first and second memory units concurrently.

10. (Currently Amended) A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of video data, the filter engine comprising:

a first memory unit operable to store blocks of video data to be processed;

a second memory unit operable to store blocks of video data to be processed;

a first shift register operable to receive and store blocks of video data from the first memory unit, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to the number of bits used to represent one pixel, said shift requiring only a single clock cycle;

a second shift register operable to receive and store blocks of video data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to the number of bits used to represent one pixel, said shift requiring only a single clock cycle; and

a processor operable to receive blocks of video data from the first and second shift registers and to perform filtering operations on blocks of video data from the first and second shift registers concurrently.

11. (Cancelled)

12. (Previously Presented) The filter engine of claim 10 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to concurrently perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and the processor is adapted to receive blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

13. (Previously Presented) The filter engine of claim 12 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor concurrently performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

14. (Previously Presented) The filter engine of claim 13 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of concurrently performing filtering operations on.

15. (Previously Presented) The filter engine of claim 10 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is concurrently performing filtering operations on a block of data received from the second shift register.

16. (Previously Presented) The filter engine of claim 15 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units concurrently performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

17. (Previously Presented) The filter engine of claim 16 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units concurrently performs filtering operations on the n most significant bits of the second shift register.

18. (Previously Presented) The filter engine of claim 17 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of concurrently performing filtering operations on.

19. (Currently Amended) A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit operable to store blocks of media data to be processed;

a second memory unit operable to store blocks of media data to be processed;

a first shift register adapted to receive and store blocks of media data from the first memory unit, wherein the first shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element, wherein said multiple is greater than 1 and said shift requires only a single clock cycle;

a second shift register operable to receive and store blocks of media data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element, wherein said multiple is greater than 1 and said shift requires only a single clock cycle; and

a processor operable to receive blocks of media data from the first and second shift registers and to perform filtering operations on blocks of media data from the first and second shift registers concurrently.

20. (Previously Presented) The filter engine of claim 19 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein the first and second shift registers are adapted to selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of one pixel.

21. (Previously Presented) The filter engine of claim 19 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to concurrently perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and the processor is adapted to receive blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

22. (Previously Presented) The filter engine of claim 21 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor concurrently performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

23. (Previously Presented) The filter engine of claim 22 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of concurrently performing filtering operations on.

24. (Previously Presented) The filter engine of claim 19 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is concurrently performing filtering operations on a block of data received from the second shift register.

25. (Previously Presented) The filter engine of claim 24 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units concurrently performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

26. (Previously Presented) The filter engine of claim 25 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units concurrently performs filtering operations on the n most significant bits of the second shift register.

27. (Previously Presented) The filter engine of claim 26 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of concurrently performing filtering operations on.